AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

monitoring processor utilization of a computer system having one or more of a processor and a power supply circuit, the processor having a plurality of performance levels;

automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a first specified time; and

automatically transitioning the processor to a next lower performance level, if any, if it is determined that the processor utilization has remained below a switch-down level for a second specified time, wherein the transitioning of the processor is initiated via a signal that is transmitted to the power supply circuit.

2. (Original) The method of claim 1, wherein the number of performance levels is two.

3. (Original) The method of claim 1, wherein the switch-up level is approximately 95% of a current processor performance level.

4. (Canceled)

5. (Currently Amended) The method of claim 1, wherein the switch-down level is approximately 95% of the next lower processor performance level.

6 – 8 (Canceled)

9. (Currently Amended) A machine-readable medium ~~that provides executable~~ having stored thereon data representing sets of instructions[[,]] which, when executed by a

~~processing system~~machine, cause ~~said processing system~~ the machine to ~~perform a method, the method comprising~~:

periodically ~~monitoring~~ monitor processor utilization of a computer system having one or more of a processor and a power supply circuit, the processor having a plurality of performance levels;

automatically ~~transitioning~~ transition the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a first specified time; and

automatically ~~transitioning~~ transition the processor to a next lower performance level, if any, if it is determined that the processor utilization has remained below a switch-down level for a second specified time, wherein the transitioning of the processor is initiated via a signal that is transmitted to the power supply circuit.

10. (Original) The machine-readable medium of claim 9, wherein the number of performance levels is two.

11. (Original) The machine-readable medium of claim 9, wherein the switch-up level is approximately 95% of a current processor performance level.

12 –13 (Canceled)

14. (Previously Presented) The machine-readable medium of claim 9, wherein the switch-down level is approximately 95% of the next lower processor performance level.

15. (Currently Amended) The machine-readable medium of claim ~~12~~9, wherein the first specified ~~period of~~ time that the processor utilization has remained above a switch-up

level to transition the processor to a higher performance level is greater than a processor-utilization monitoring period.

16. (Previously Presented) The machine-readable medium of claim 15, wherein the specified period of time that the processor utilization has remained below a switch-down level to transition the processor to a next lower performance level is equal to the processor-utilization monitoring period.

17. (Previously Presented) The method of claim 1 wherein the first specified time is greater than the second specified time.

18. (Previously Presented) The method of claim 1 wherein the second specified time is greater than the first specified time.

19. (Previously Presented) The machine-readable medium of claim 9 wherein the first specified time is greater than the second specified time.

20. (Previously Presented) The machine-readable medium of claim 9 wherein the second specified time is greater than the first specified time.

21. (New) A system comprising:

a processor including a power management system (PMS) to

monitor processor utilization, wherein the processor has a plurality of performance levels,

automatically transition the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a first specified time, and

automatically transition the processor to a next lower performance level, if any, if it is determined that the processor utilization has remained below a switch-down level for a second specified time;

a power supply coupled to the processor;

a power supply circuit coupled to the power supply; and

an input/output (I/O) controller coupled to the power supply circuit, the I/O controller to transmit a signal to the power supply circuit to initiate the transitioning of the processor.

22. (New) The system of claim 21, wherein the switch-up level is approximately 95% of a current processor performance level.

23. (New) The system of claim 21, wherein the switch-down level is approximately 95% of the next lower processor performance level.